# CHEN Zi Hang

*The Hong Kong University of Science and Technology (Guangzhou)*

zchen097@connect.hkust-gz.edu.cn | github.com/maxkev1n

## Personal Profile

A second year microelectronics PhD student at The Hong Kong University of Science and Technology (Guangzhou), undertaking the computer architecture, computer system, machine learning. Zealous about computer architecture and with 3+ years of experience specialising in computer architecture simulators (gem5, gpgpusim and mgpusim), Verilog development, high performance RISC-V CPU processor (Xiangshan RISC-V processors), machine learning framework (pytorch).

## Education

**Nanjing University of Science and Technology** *Nanjing, China*

B.S. in Computer Science and Technology *Sept 2019 - June 2023*

- Leader of the school team of NSCSCC(National Student Computer System Capability Challenge) 2021
- Leader of a school research project about *pipeline RISC-V processor*
- Working as a teaching assistant for MIPS CPU Design in autumn 2021 and autumn 2022

**The Hong Kong University of Science and Technology (Guangzhou)** *Guangzhou, China*

Doctor of Philosophy in Microelectronics (expected) *Sept 2023 - current*

- Spending 8+ months on GPU architecture, especially simulators like gpgpusim and mgpusim.
- Working on machine learning frameworks and lossy compression techniques.

## Work Experience

**The Hong Kong University of Science and Technology (Guangzhou)**

Research Assistant *Feb 2023 - Aug 2023*

- Focus on GPGPU architecture.
- **Technical Skills:** MGPUSim, Opencl, Golang.

**Institute of Computing Technology, Chinese Academy of Sciences**

Research Assistant *March 2022 - May 2021*

- Received a comprehensive and general training on computer architecture and computer system.
- Learned basic operations on GEM5(a sophisticated system simulator), including configure a out of order processor, run benchmarks and workloads, measure more useful metrics
- Add some functions to the NEMU(Nanjing university Emulator), exploit NEMU to generate some workloads and checkpoints, run RISC-V version of Linux on NEMU
- **Technical Skills:** GEM5, NEMU, QEMU, Python, C++, C, Ubuntu Linux, Linux tools, Git, Bash.

**Beijing Institute of Open Source Chip**

Intern *June 2022 - Feb 2023*

- Tested simpoint profiling on NEMU and generated checkpoints of special workloads.
- collaborated to implement two outstanding functions called *difftest* and *GCPT restorer* on GEM5.
- explored a new technique called *speculative renaming* on GEM5
- collaborated to implement a new microarchitecture called *decoupled frontend* on GEM5, which is combined with a *loop detector*, a *TAGE predictor* and a *next stream predictor*
- Aligning the GEM5 with Nanhu(2nd XiangShan processor) microarchitecture
- **Technical Skills:** GEM5, NEMU, C++, C, Python, Ubuntu Linux, Git, Zsh.

**Nanjing University of Science and Technology**

Teaching Assistant *November 2021 & August 2022*

- Taught a courser called MIPS CPU design that students need to design their own MIPS processor.
- prepared teaching materials including slides and guidelines
- solved students' related problems and checked students' lab's results and projects

## Skills

**Programming** C/C++, Java, Golang, Python, HTML/CSS, SQL, Verilog.

**Miscellaneous** Ubuntu Linux, Shell (Bash/Zsh), LaTeX, Markdown, Git, Vivado, GEM5, GPGPUSim, MGPUSim.